

FIG. 3

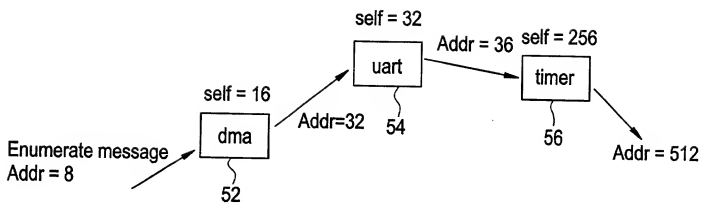


FIG. 4

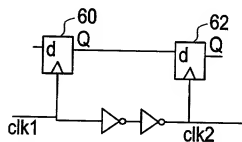


FIG. 5

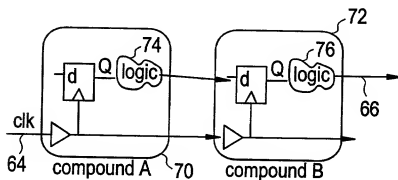


FIG. 6

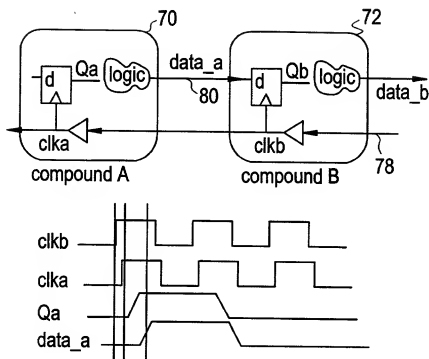
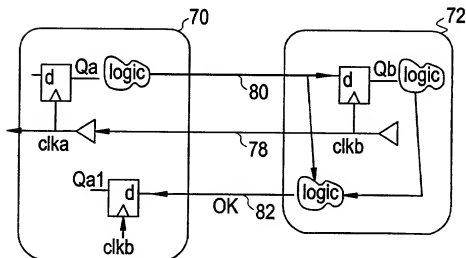
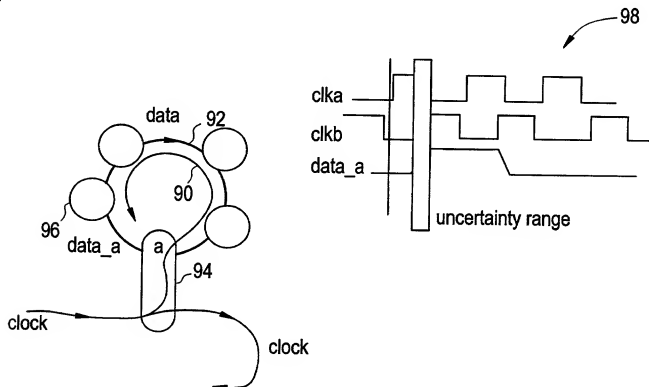


FIG. 7



[illegible]

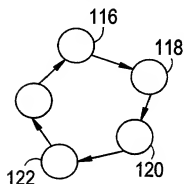


FIG. 13

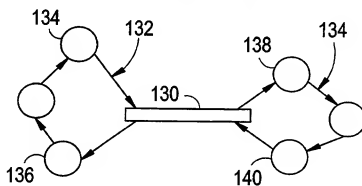


FIG. 14

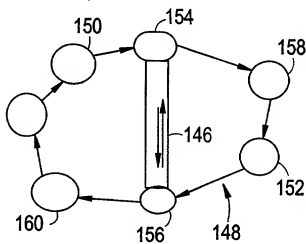


FIG. 15

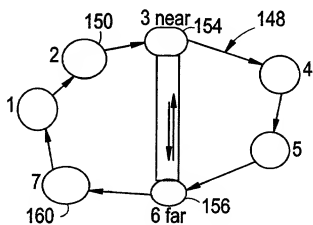


FIG. 16

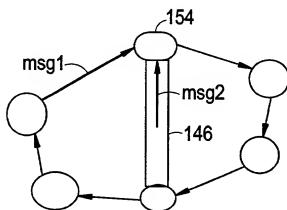


FIG. 17

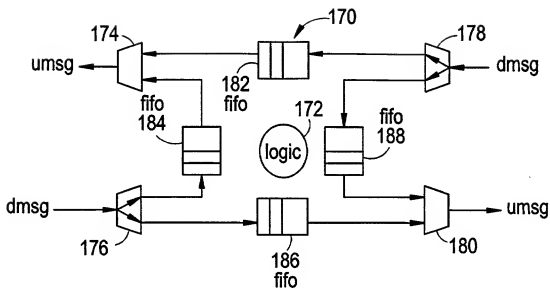


FIG. 18

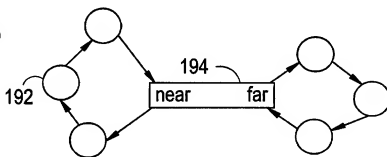
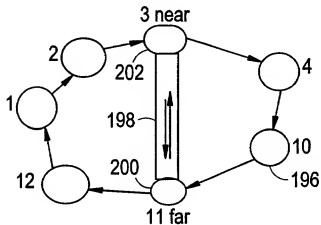


FIG. 19



2004370-000001

FIG. 20

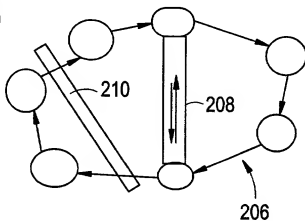


FIG. 21

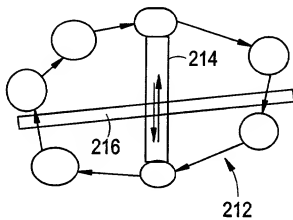
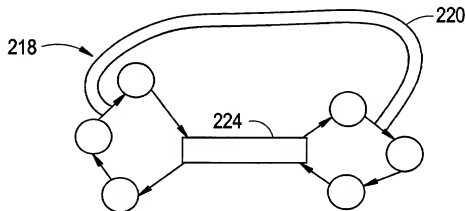


FIG. 22





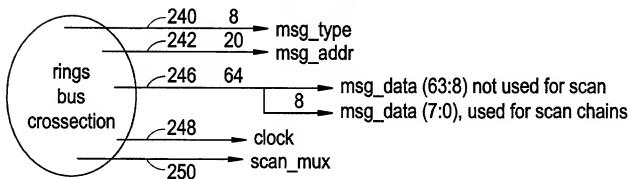


FIG. 26

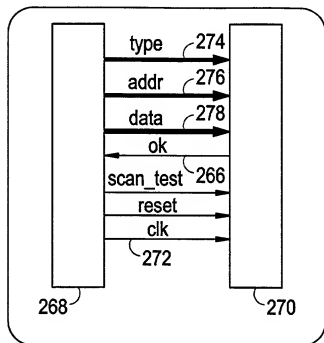


FIG. 27

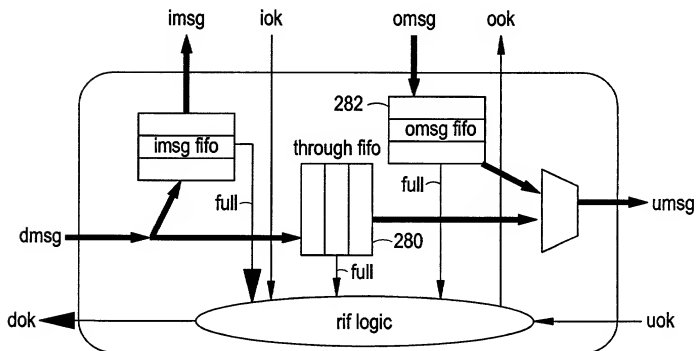




FIG. 29

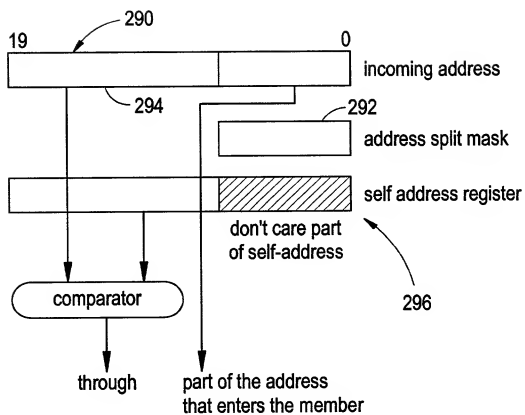


FIG. 30

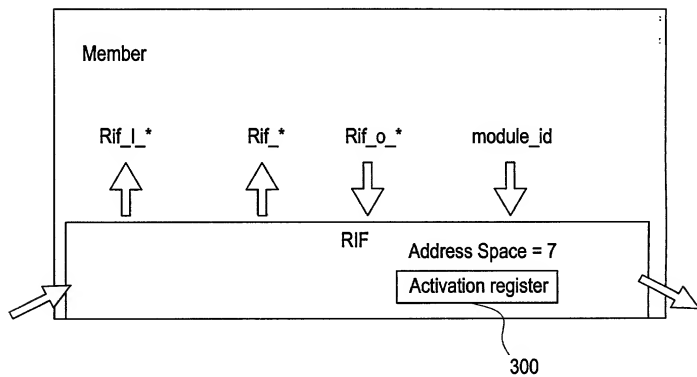


FIG. 31

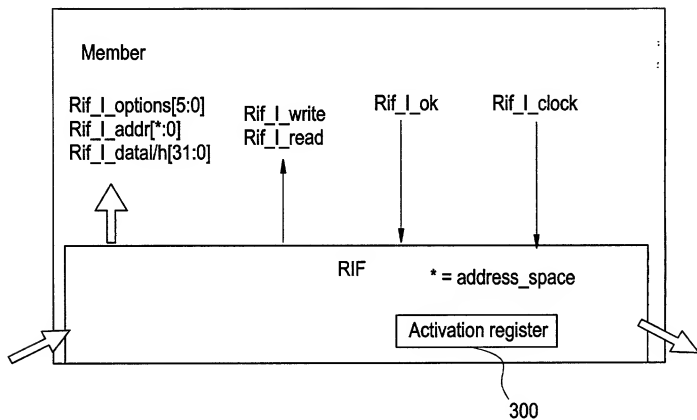


FIG. 32

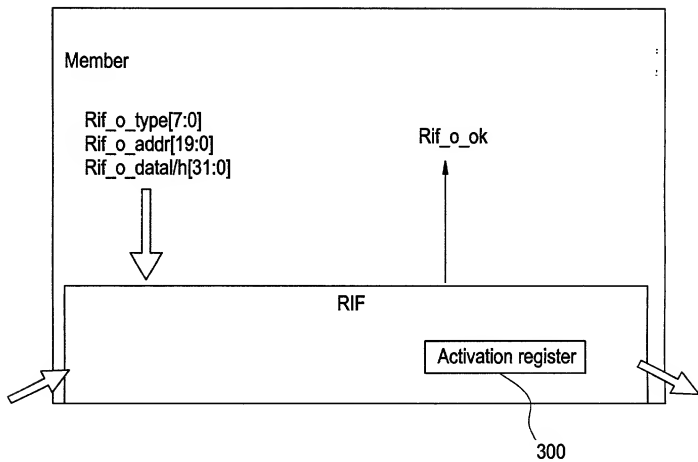


FIG. 33

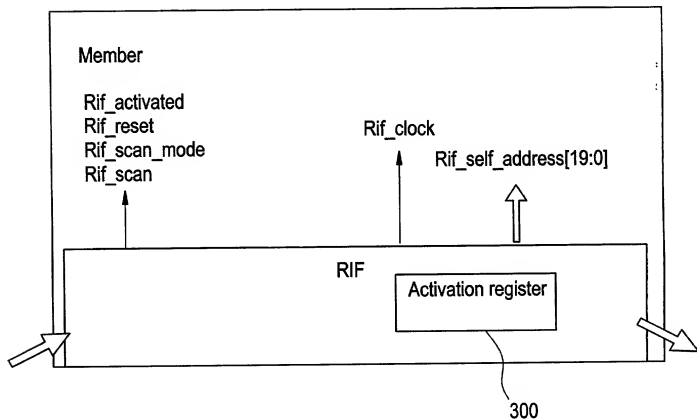




FIG. 34

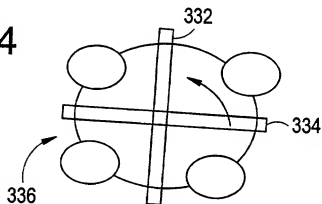


FIG. 35

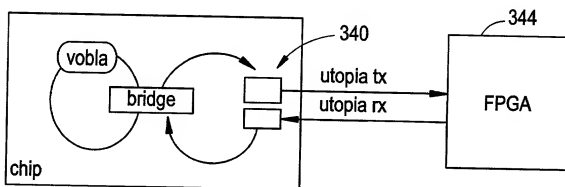


FIG. 36

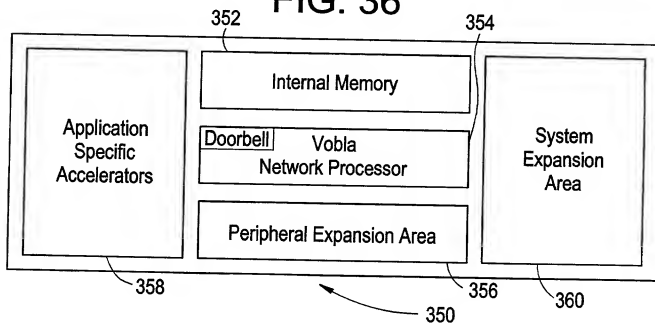
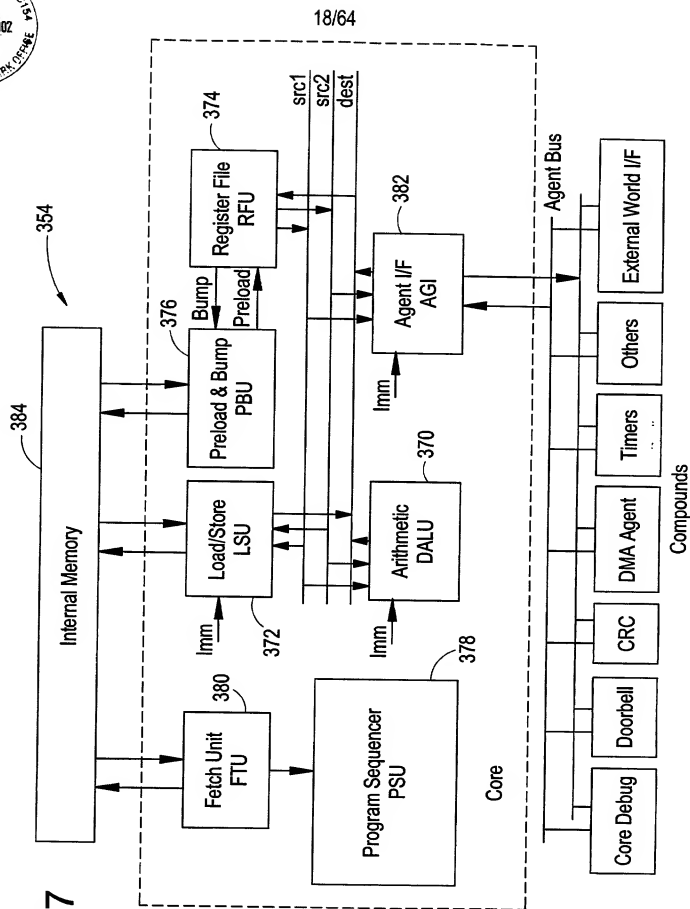


FIG. 37



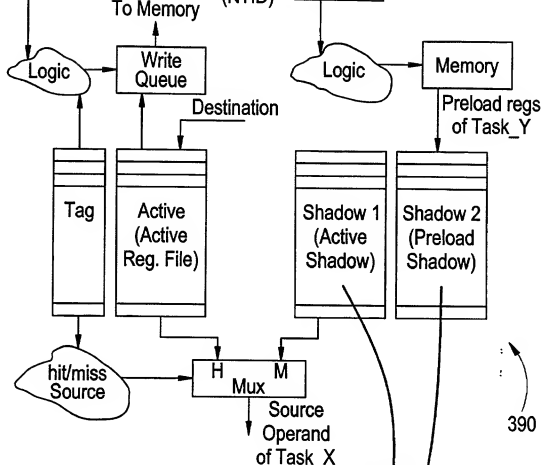
Current Task  
(CTID)

Task\_X

Next Task  
(NTID)

### Task Y

FIG. 38



### After a task switch

Current Task  
(CTID)

Task\_Y

## To Memory

Next Task  
(NTID)

### Task\_Z

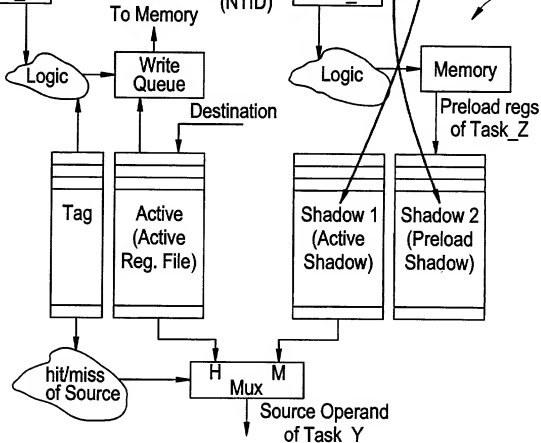


FIG. 39

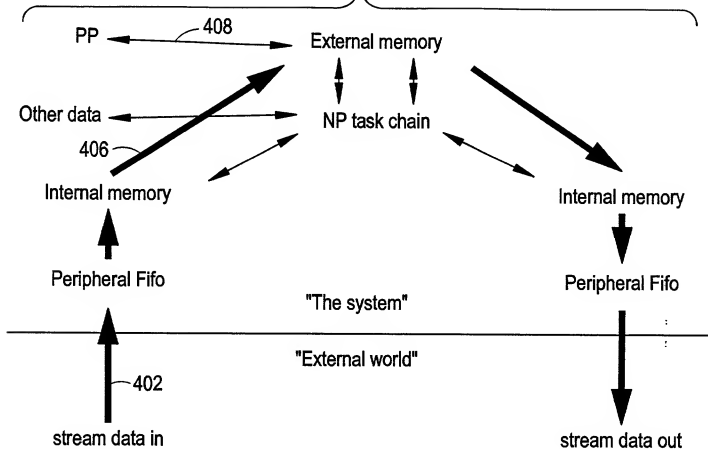


FIG. 40

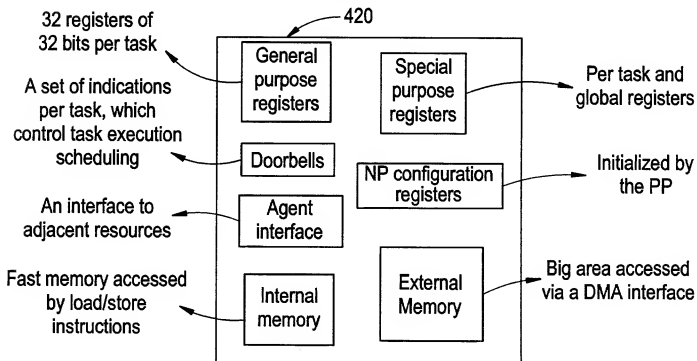
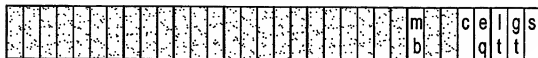


FIG. 41

R1 register

3 3 2 2 2 2 2 2 2 2 2 2 1 1 1 1 1 1 1 1 1 1 9 8 7 6 5 4 3 2 1 0  
1 0 9 8 7 6 5 4 3 2 1 0 9 8 7 6 5 4 3 2 1 0



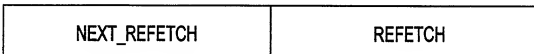
s - sticky bit  
 eq - equal/zero  
 lt - less then/negative  
 gt - greater then/positive  
 c - carry  
 mb - reflection of the RAM mult-reader busy indication

430

FIG. 42

3 3 2 2 2 2 2 2 2 2 2 2 1 1 1 1 1 1 1 1 1 1 9 8 7 6 5 4 3 2 1 0  
1 0 9 8 7 6 5 4 3 2 1 0 9 8 7 6 5 4 3 2 1 0

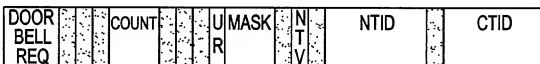
REFETCH SPR  
(spr index - 0)



440

3 3 2 2 2 2 2 2 2 2 2 2 1 1 1 1 1 1 1 1 1 1 9 8 7 6 5 4 3 2 1 0  
1 0 9 8 7 6 5 4 3 2 1 0 9 8 7 6 5 4 3 2 1 0

TASK SPR  
(spr index - 1)



442

3 3 2 2 2 2 2 2 2 2 2 2 1 1 1 1 1 1 1 1 1 1 9 8 7 6 5 4 3 2 1 0  
1 0 9 8 7 6 5 4 3 2 1 0 9 8 7 6 5 4 3 2 1 0

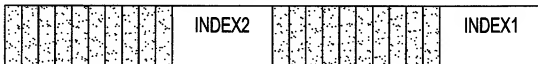
TRAP SPR  
(spr index - 2)



444

3 3 2 2 2 2 2 2 2 2 2 2 1 1 1 1 1 1 1 1 1 1 9 8 7 6 5 4 3 2 1 0  
1 0 9 8 7 6 5 4 3 2 1 0 9 8 7 6 5 4 3 2 1 0

MINDEX SPR  
(spr index - 3)



446

FIG. 43

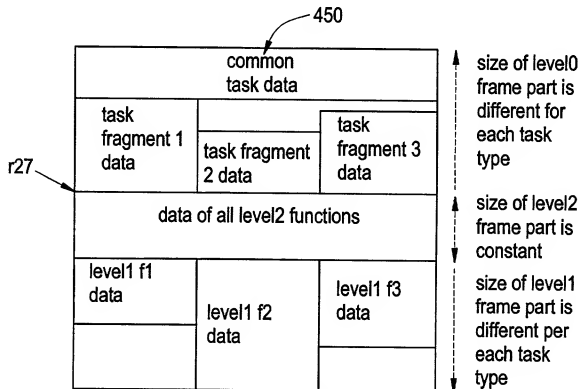
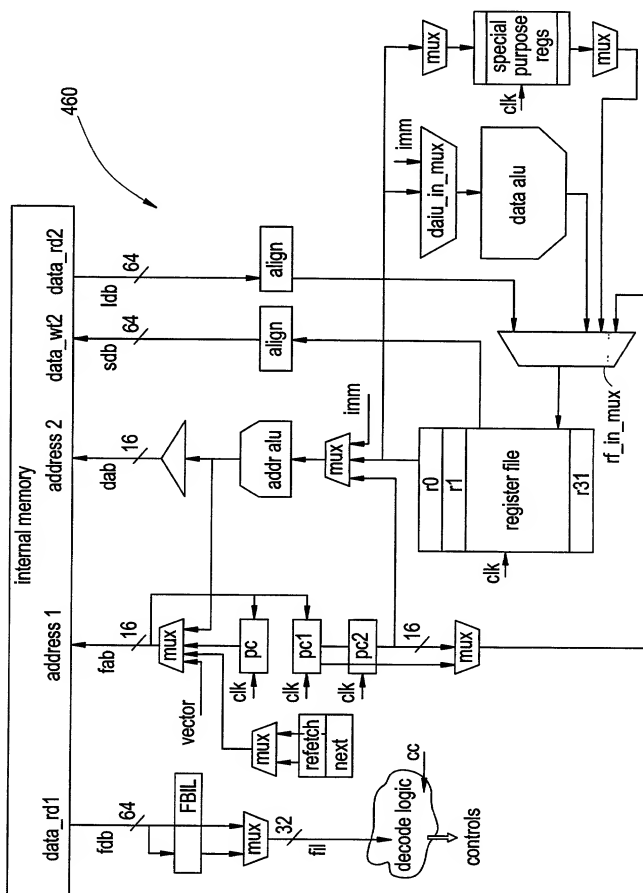
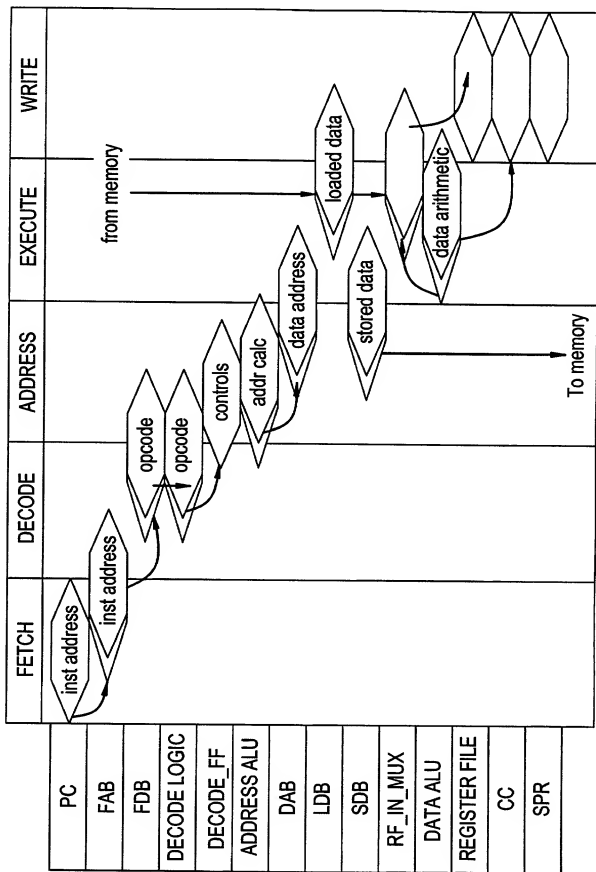


FIG. 44



**FIG. 45**



- Flip Flop      - Logic



FIG. 46

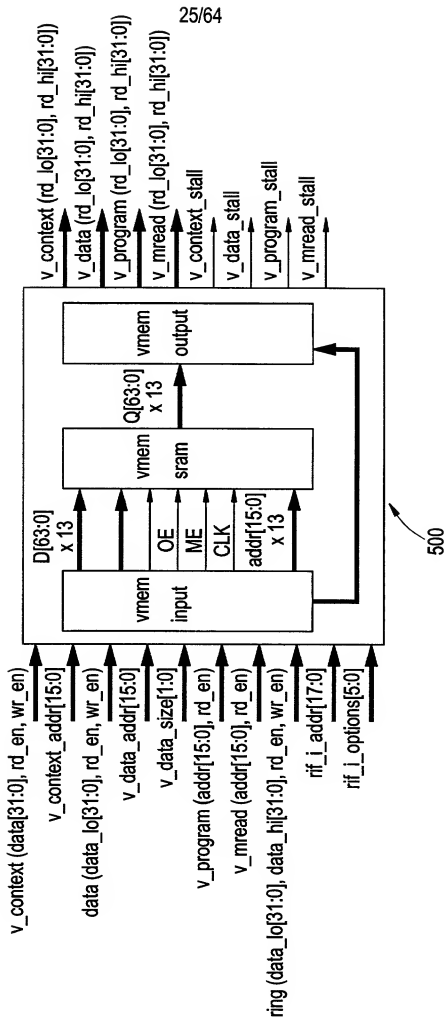


FIG. 47

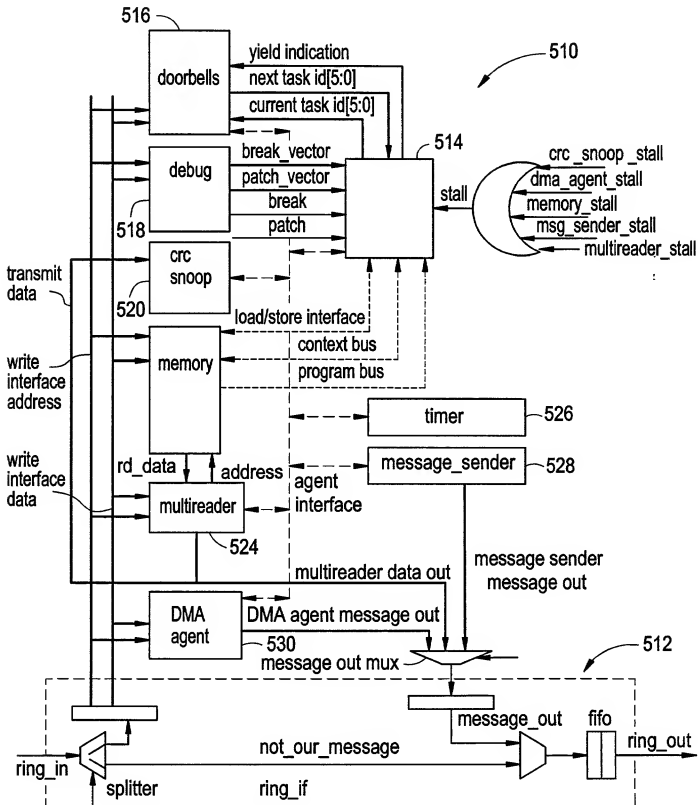


FIG. 48

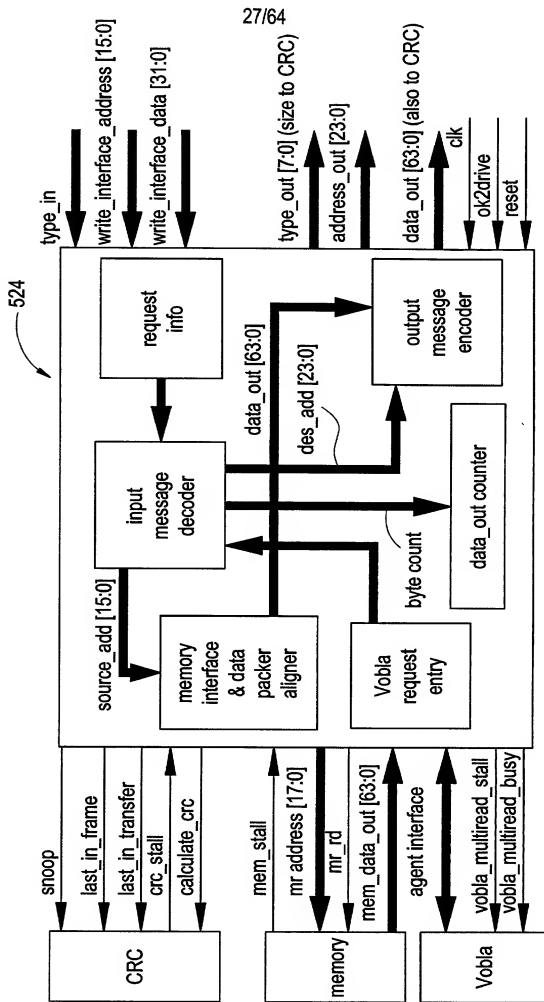


FIG. 49

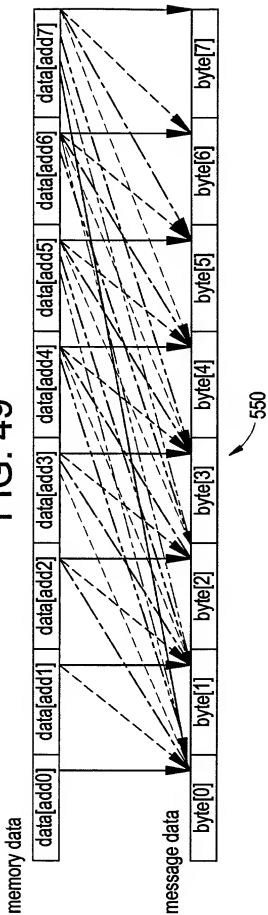


FIG. 50

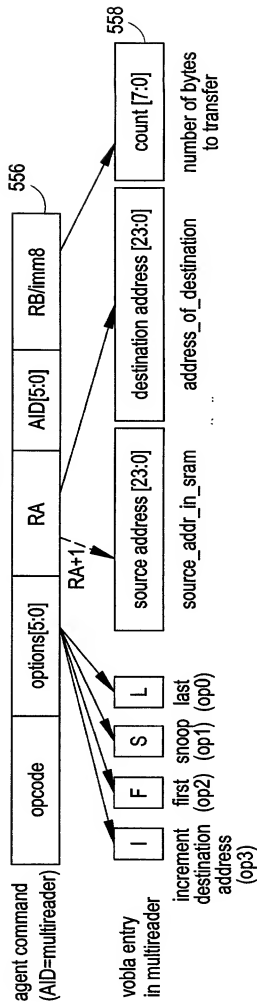


FIG. 51

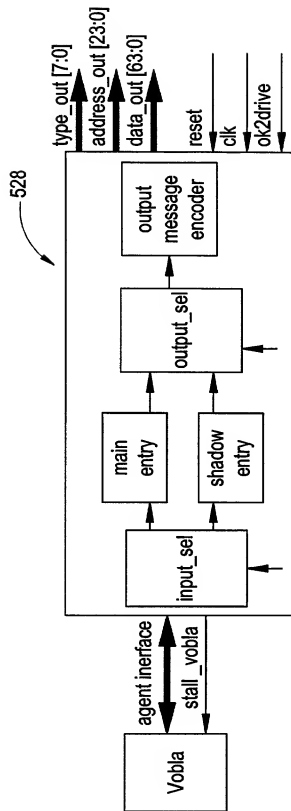


FIG. 52

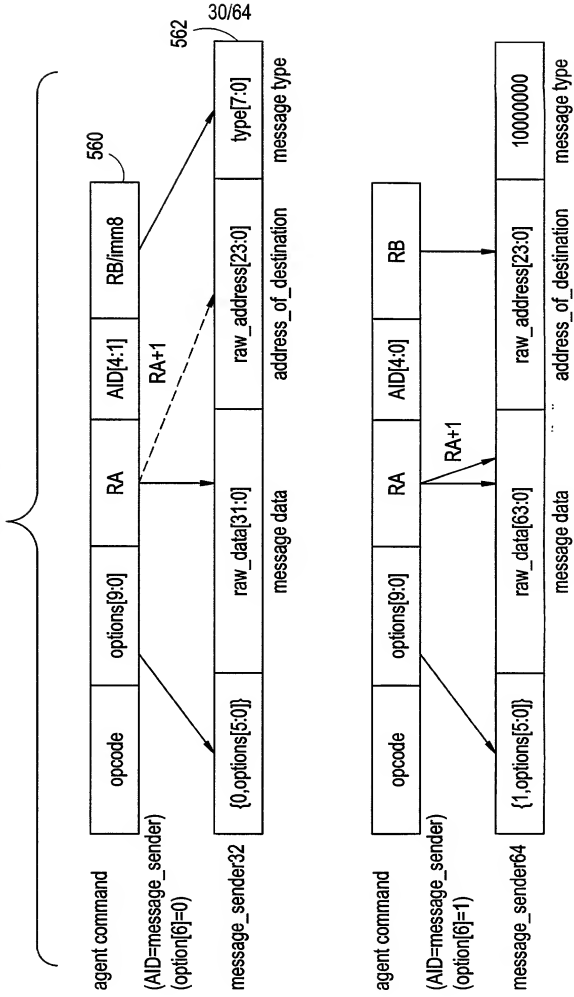


FIG. 53

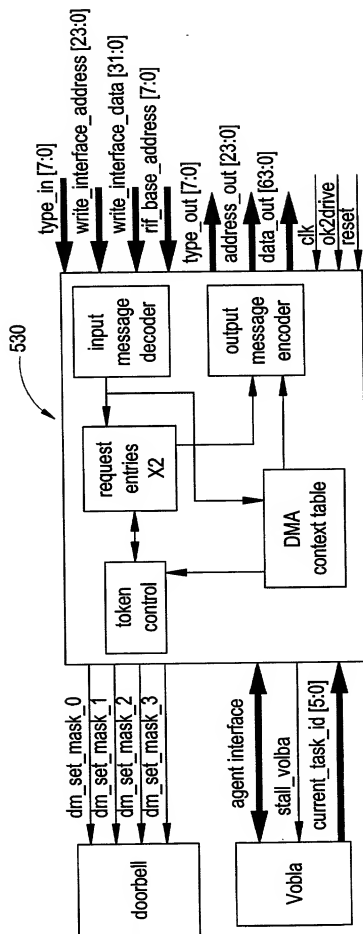


Figure 1 is a detailed block diagram of the DMA request entry. The entry is a 32/64-bit structure. It is divided into several fields: opcode, agent command (AID=dma agent) [10:0], options [10:0], RA, AID[4:0], RB/imm8, and a 576-bit field. The options field is further divided into M (modify address (OP9)), U (urgent (OP2)), D (dir set (OP1)), A (auto set (OP0)), NA (send ack (OP3)), and L (long address (OP10)). The RA field points to a dram address [31:0]. The AID[4:0] field points to a dram address [23:0]. The RB/imm8 field points to a dram address [7:0]. The 576-bit field is divided into a count [7:0] and a number of bytes to transfer or address modifier.



FIG. 55

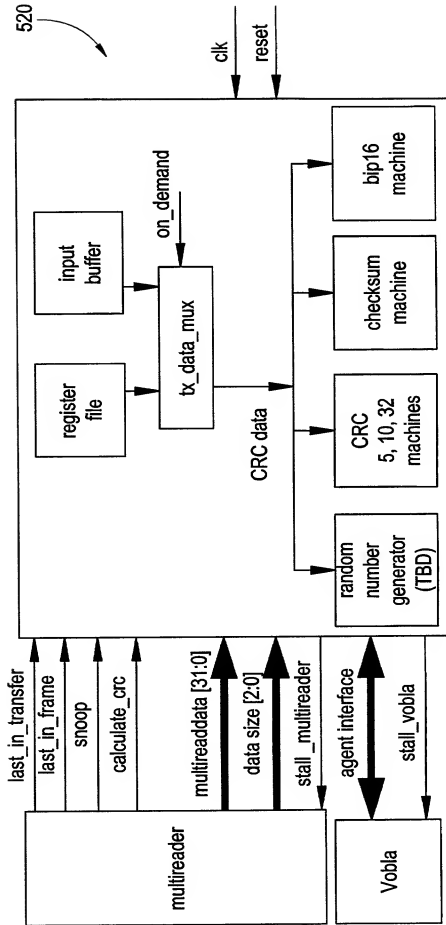


FIG. 56

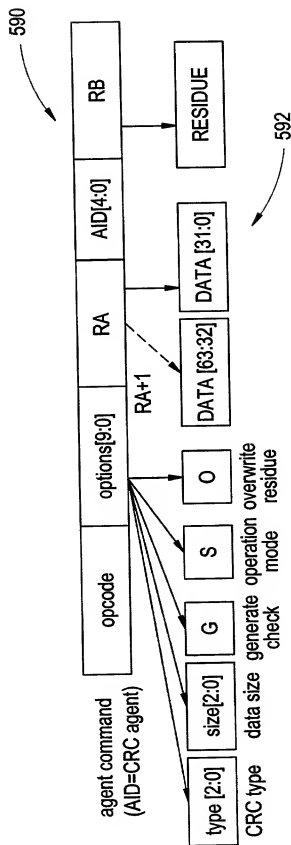


FIG. 57

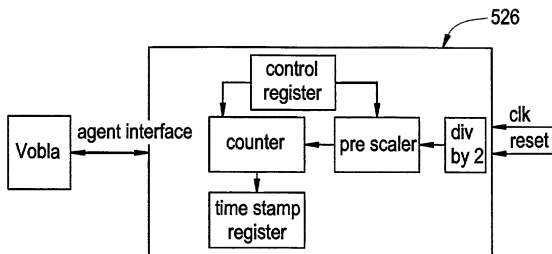
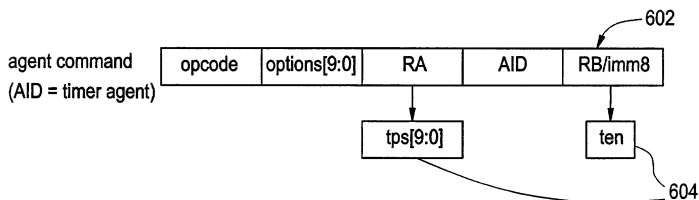


FIG. 58



516

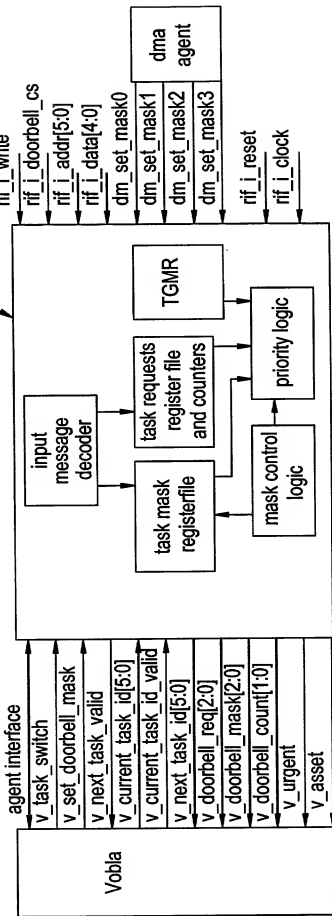
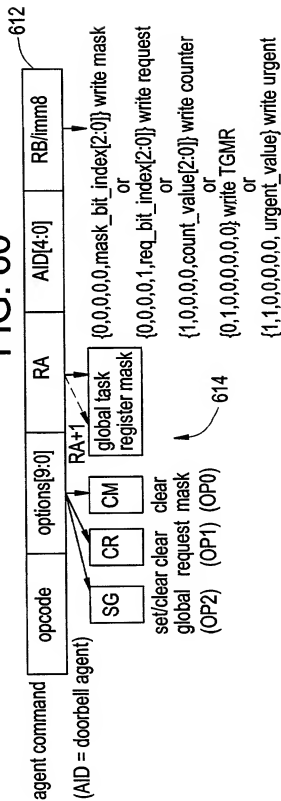


FIG. 60



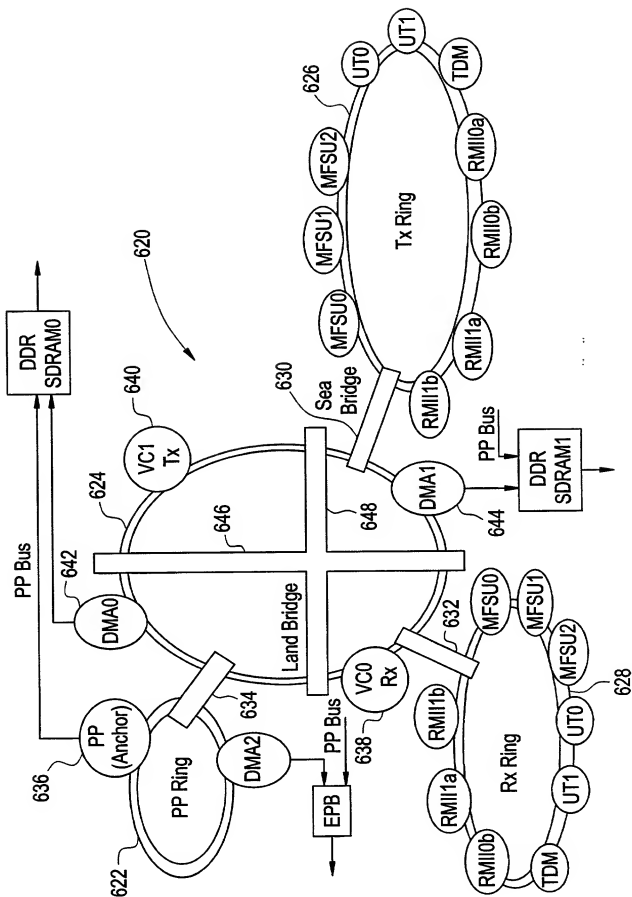
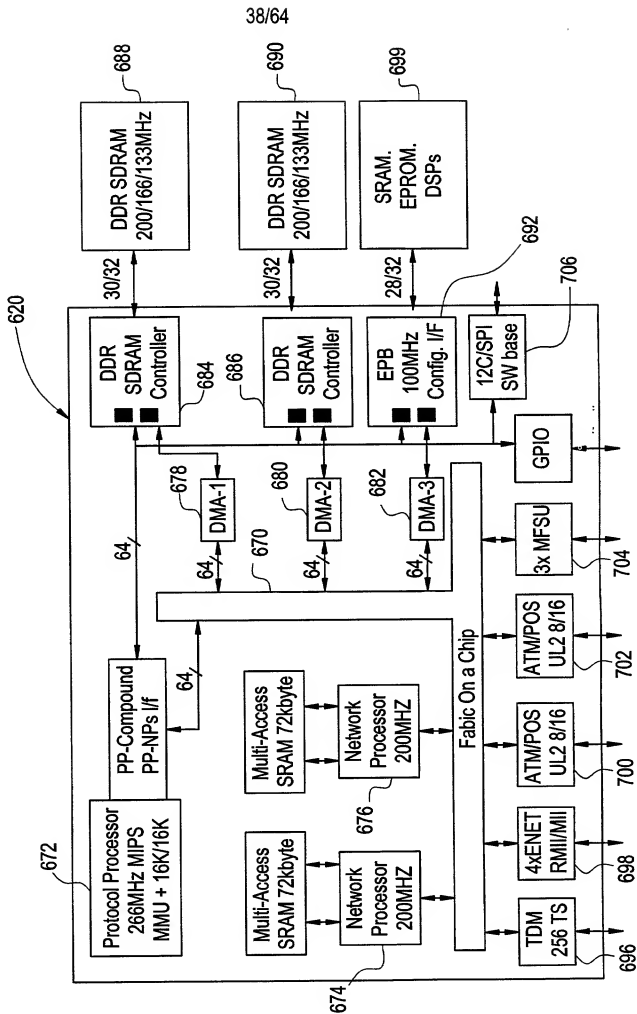


FIG. 62



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FIG. 63

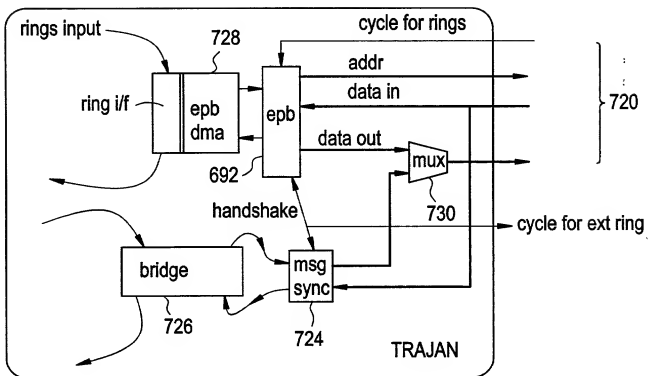
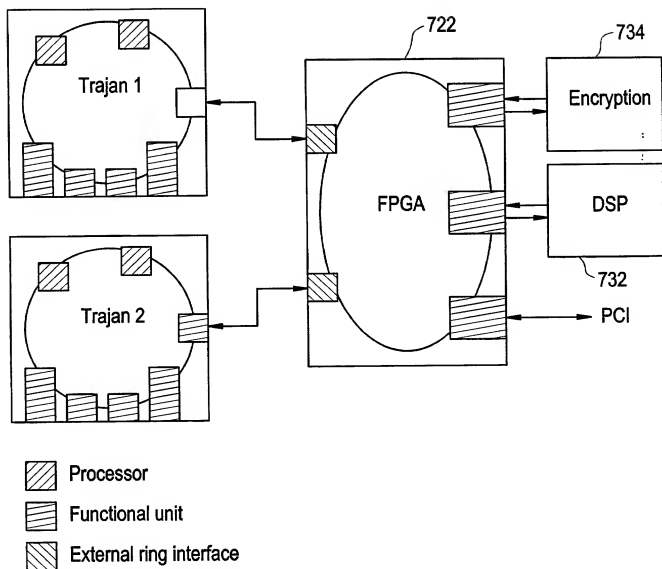


FIG. 64



10061730-092602



FIG. 65

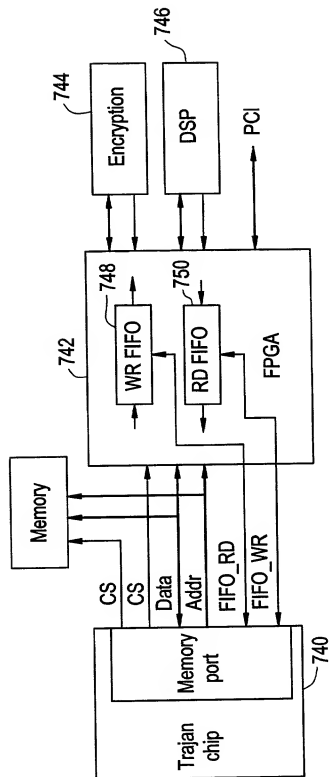


FIG. 66

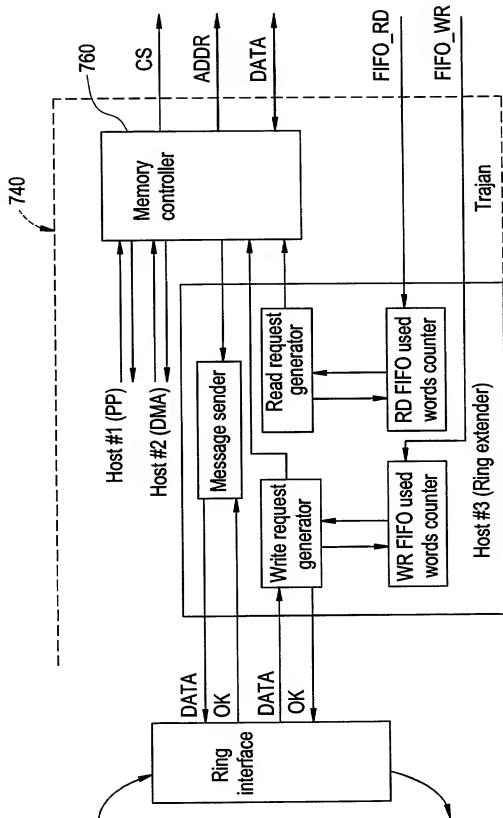


FIG. 67

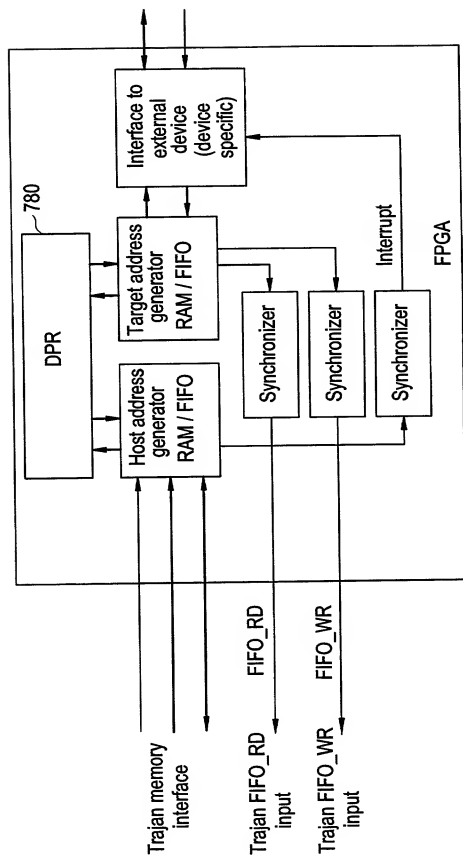


FIG. 68

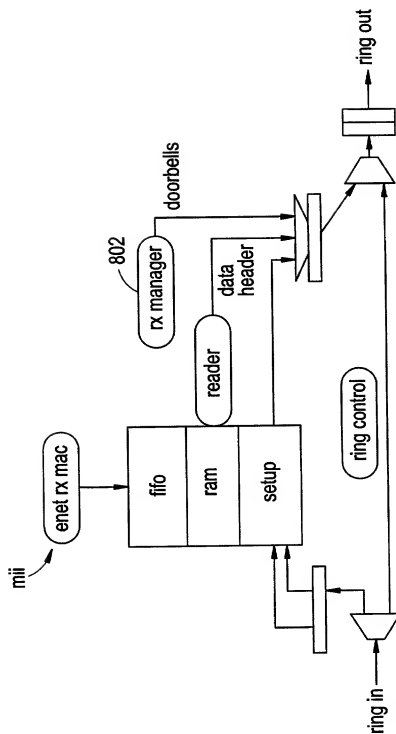


FIG. 69

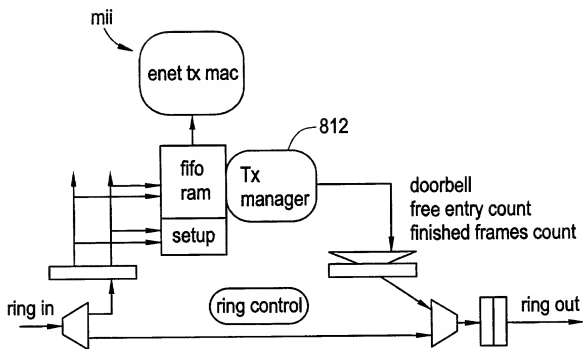


FIG. 70

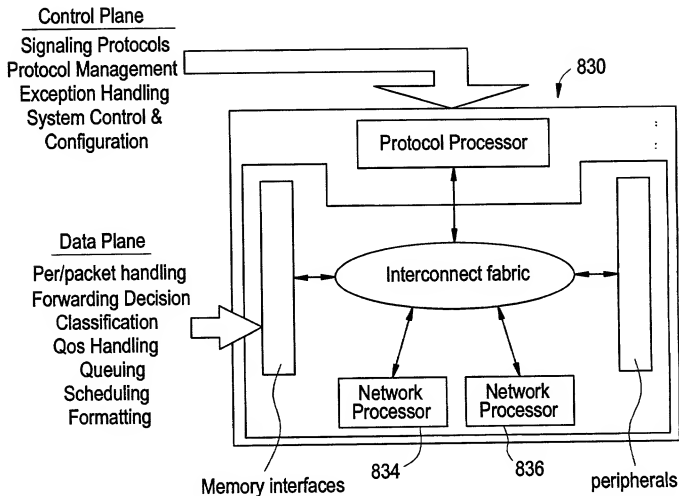


FIG. 71

840

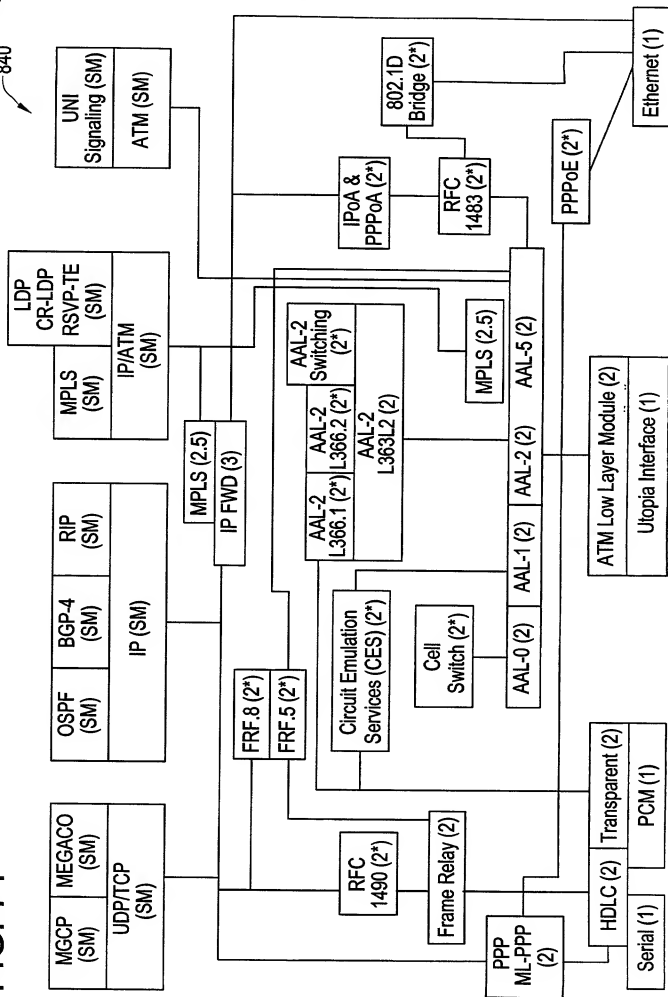


FIG. 72

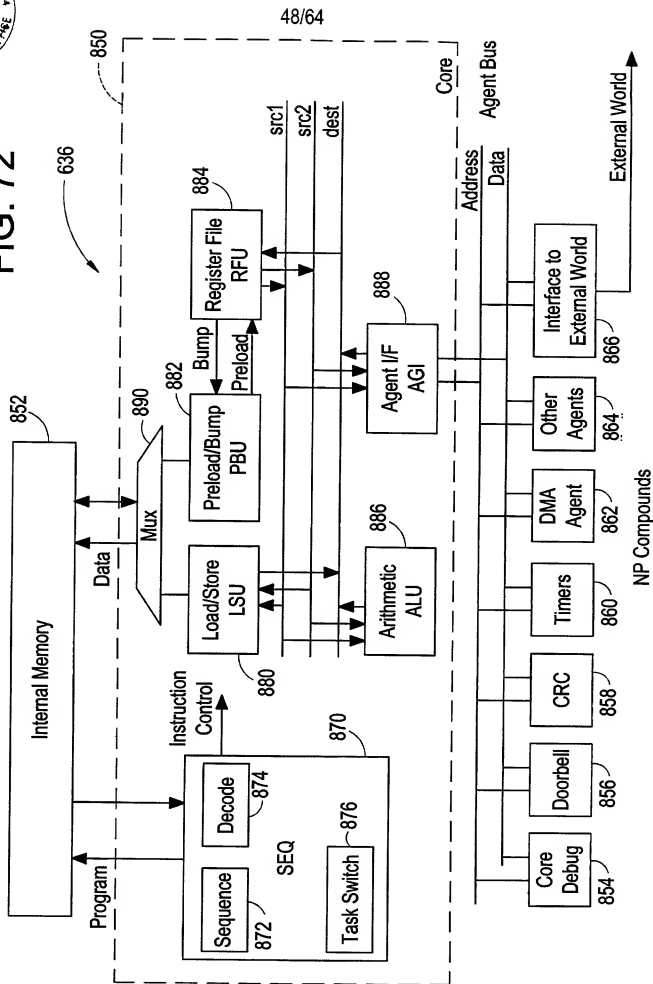




FIG. 73

900

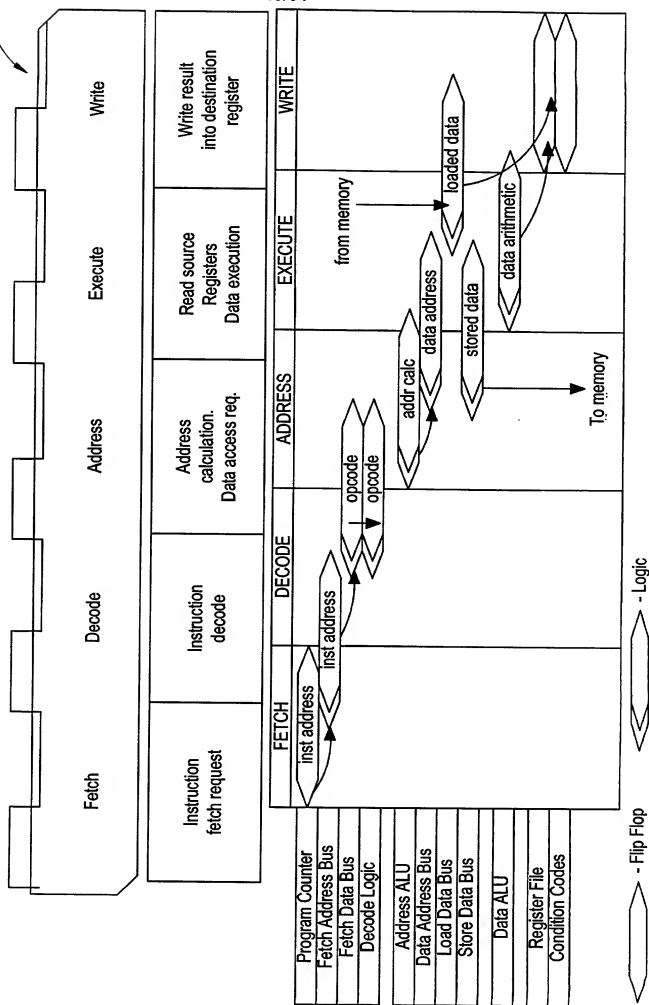


FIG. 74

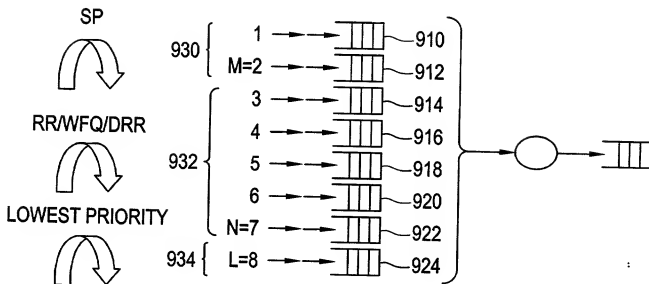


FIG. 75

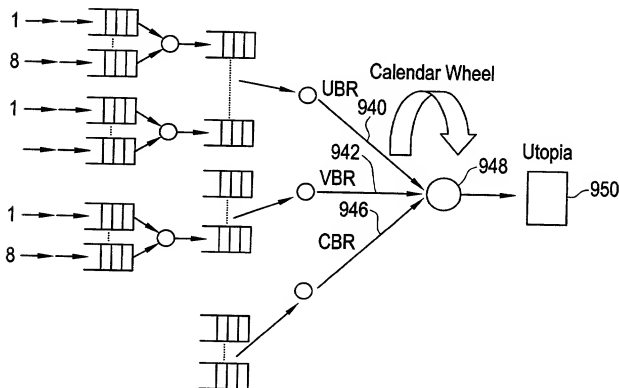


FIG. 76

960

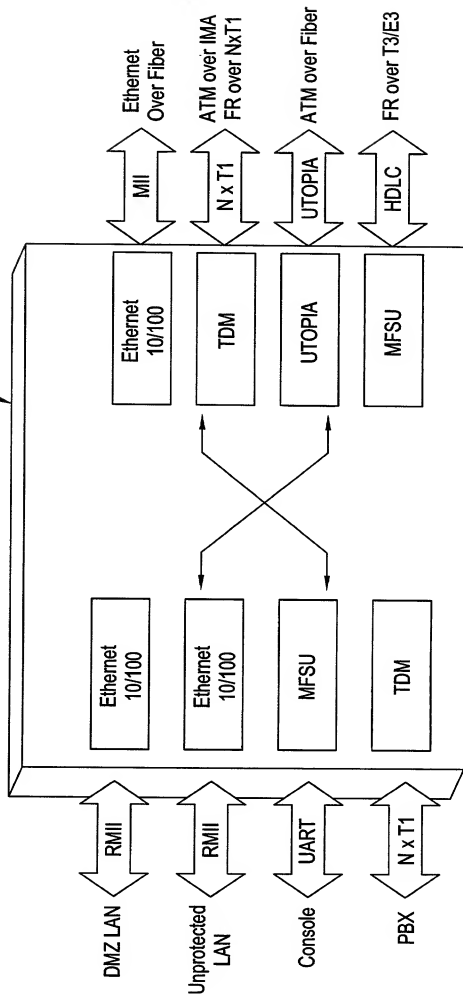


FIG. 77

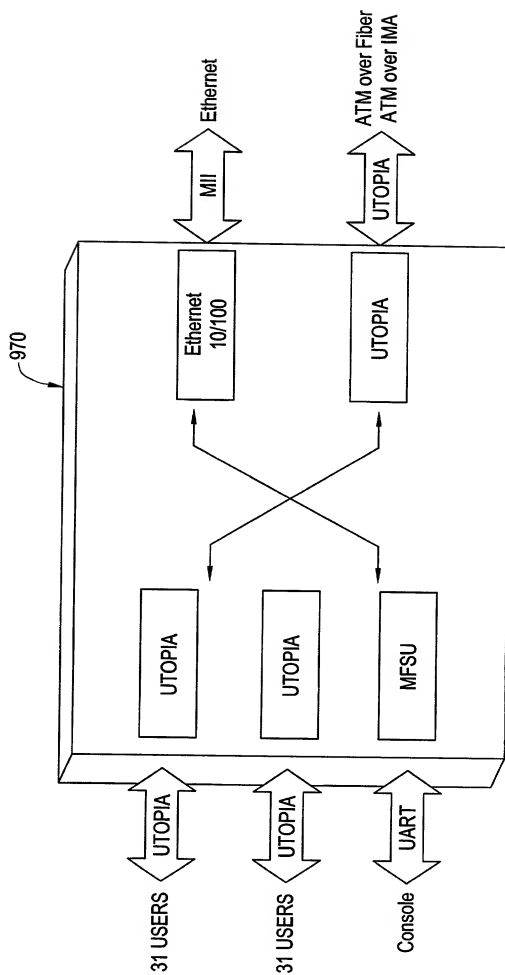


FIG. 78

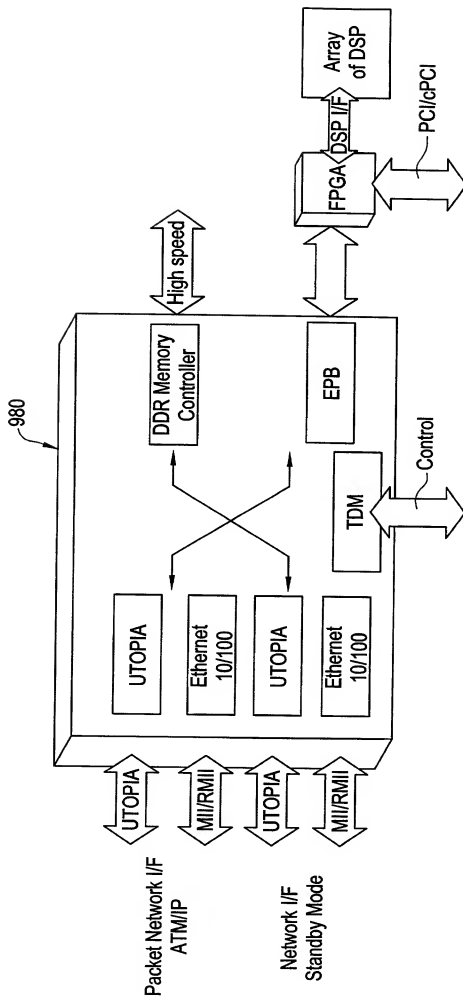


FIG. 79

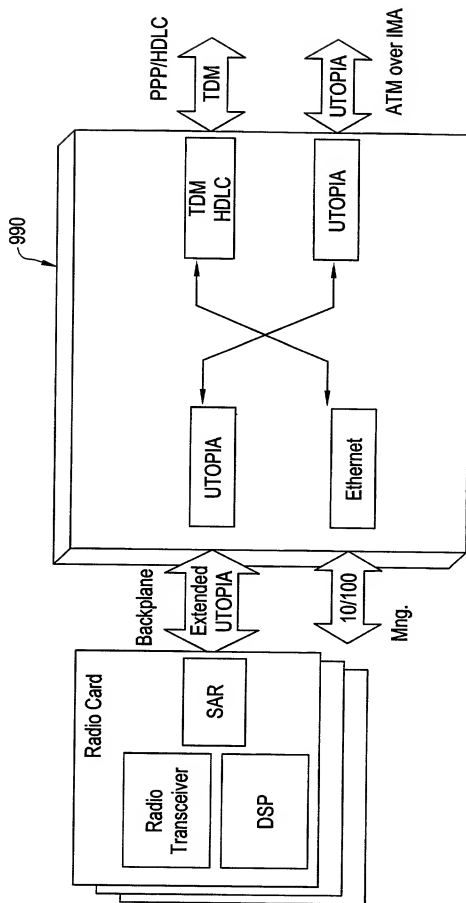


FIG. 80

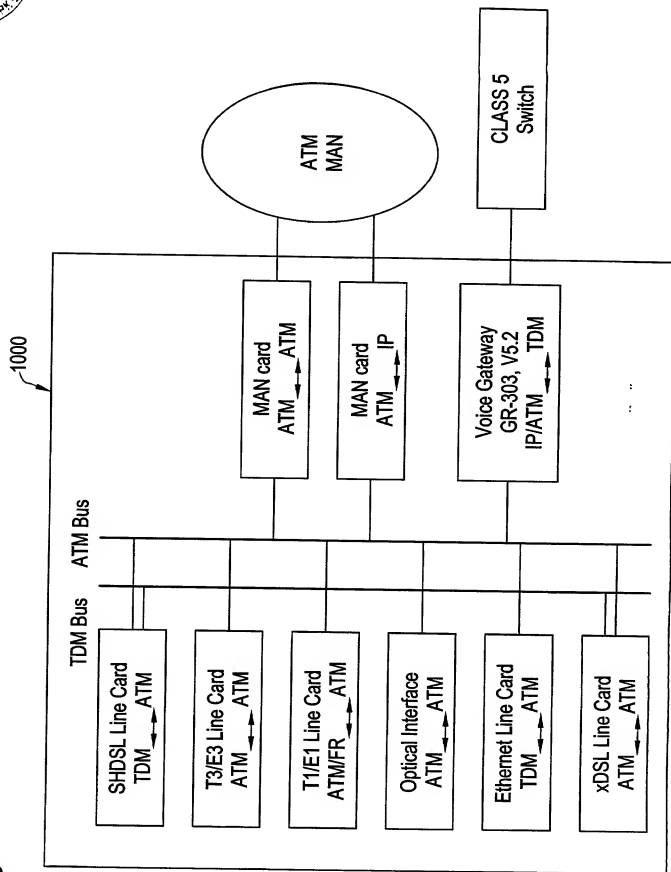


FIG. 81

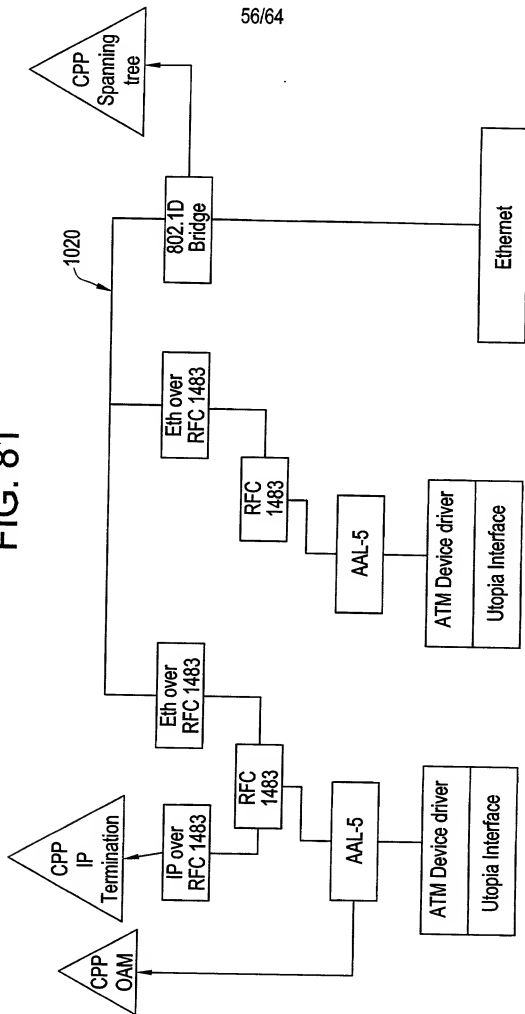




FIG. 82

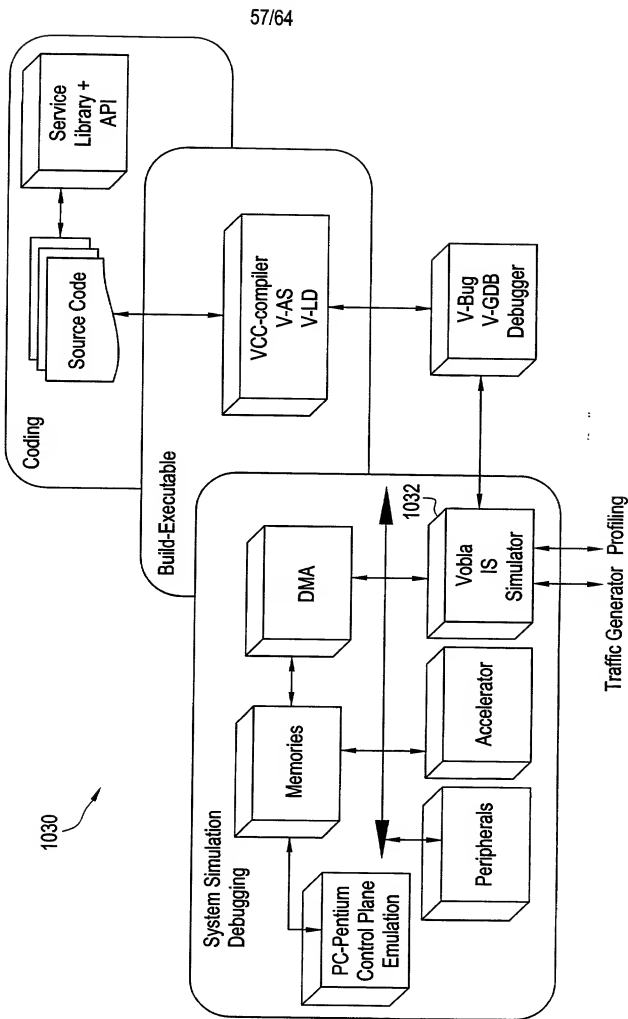


FIG. 83

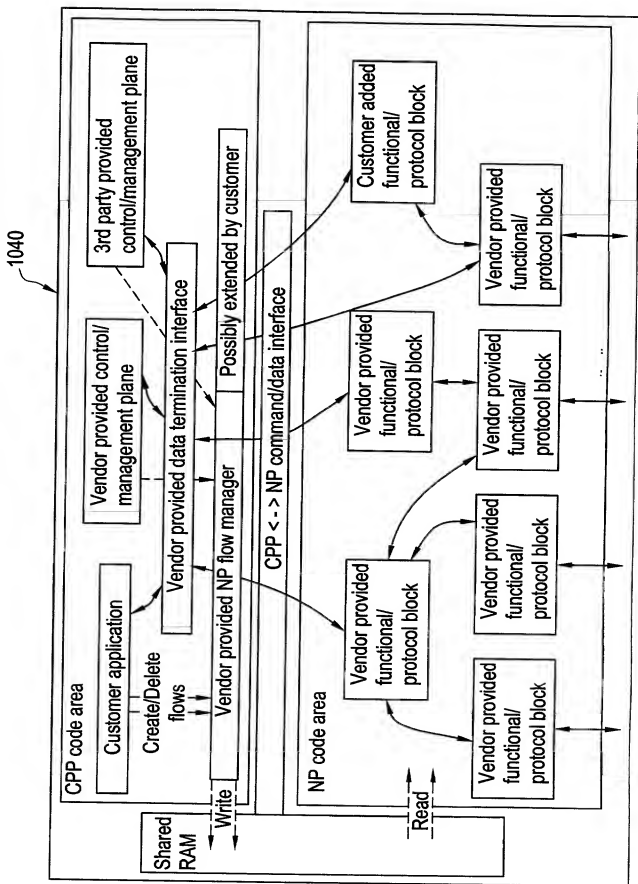
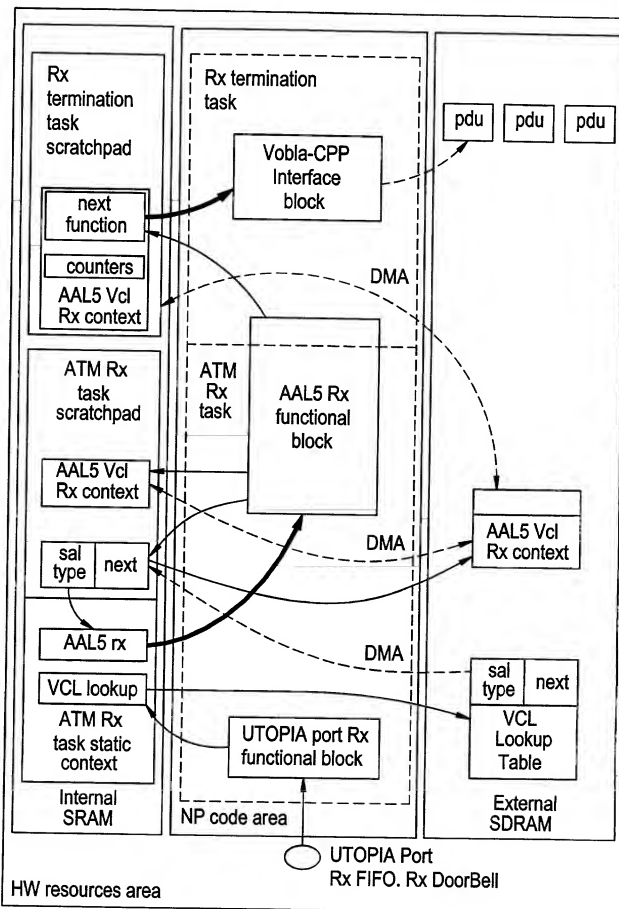


FIG. 84

1050



FORWARDED BY DESIG

FIG. 85

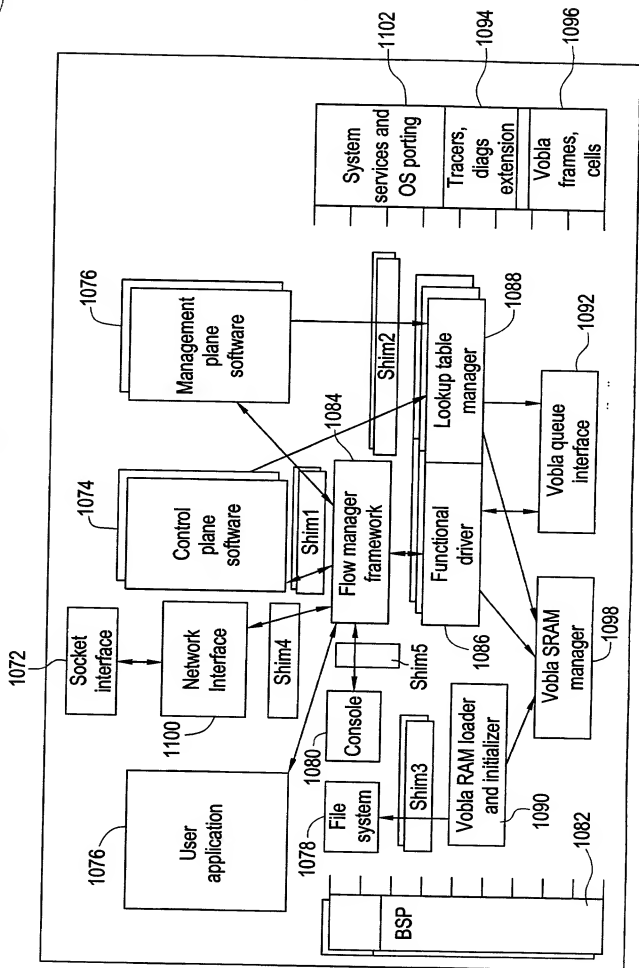
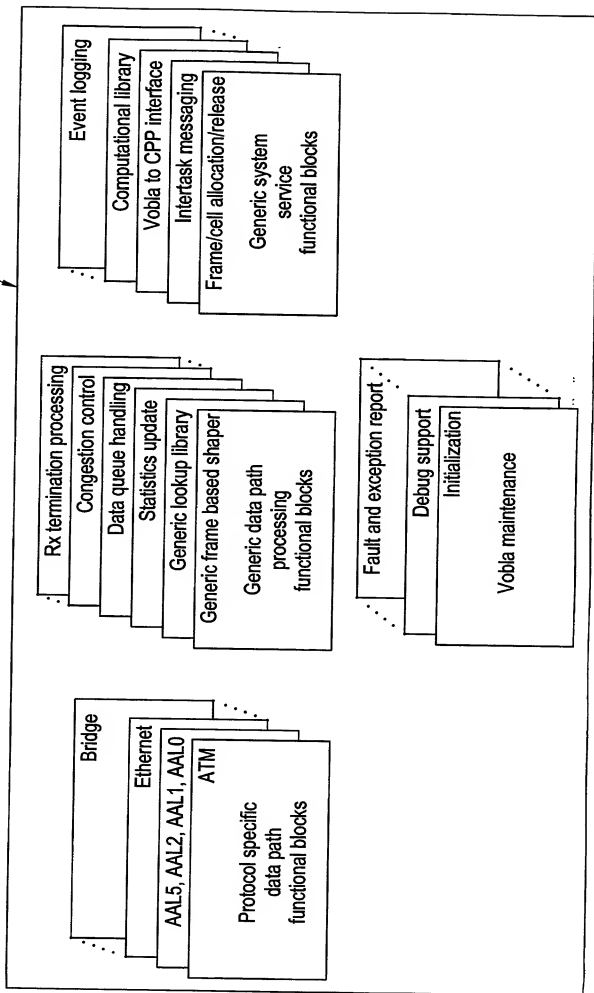


FIG. 86

1200

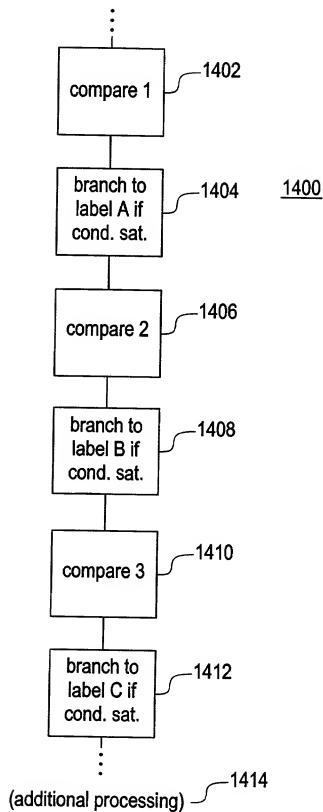




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# FIG. 87

PRIOR ART



20020926 005149001

FIG. 88

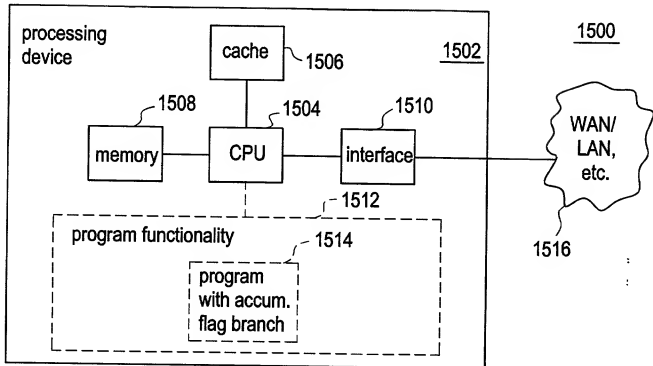
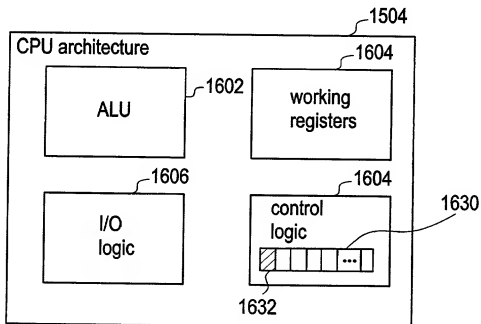


FIG. 89





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FIG. 90

